IDEC Chip Design Contest

Timing-Skew Detect and Compensation Technique for Time-Interleaved ADC

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Introduction

Ultra-wideband (UWB) wireless communication is one of the contributors to the prosperity of the IoT and is also one of the representative beneficiaries that is keeping to evolve with IoT. With continuing development of UWB wireless communications, the demand for multi-GS/s high-speed and medium-resolution ADCs have been increasing. To meet this demand, people apply time-interleaved architecture to the SAR ADC. Unfortunately, time-interleaved SAR ADCs have a critical sampling timing skew drawback. Calibrating this timing skew is very challenging, because the errors strongly depend on the input frequencies. Fig. 1 shows the basic structure and timing-diagram of the TI ADC which consists of N number of sub-ADCs.

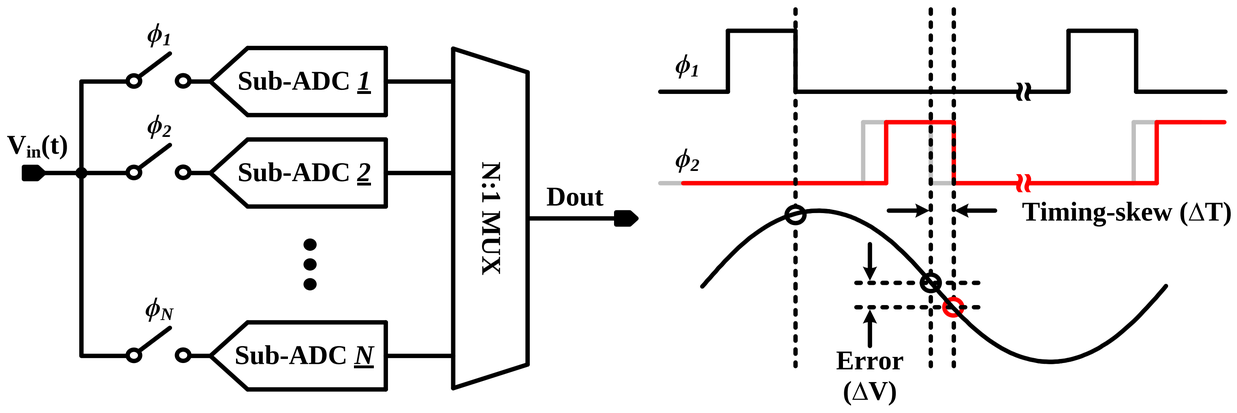

Fig. 1. Basic structure of the TI ADC and its timing-diagram.

Window Detector-based Timing-Skew Detection

More recently, the timing-skew calibration technique using window detector was proposed. In this technique, the timing-skew information can be obtained by monitoring each sub-ADC's outputs corresponding to the input within the window region set near zero-crossing as shown in Fig. 2. And the timing-skew can be calibrated by minimizing the mean absolute value of each sub-ADC's outputs. So, it is important to detect whether the input is in the window region or not.

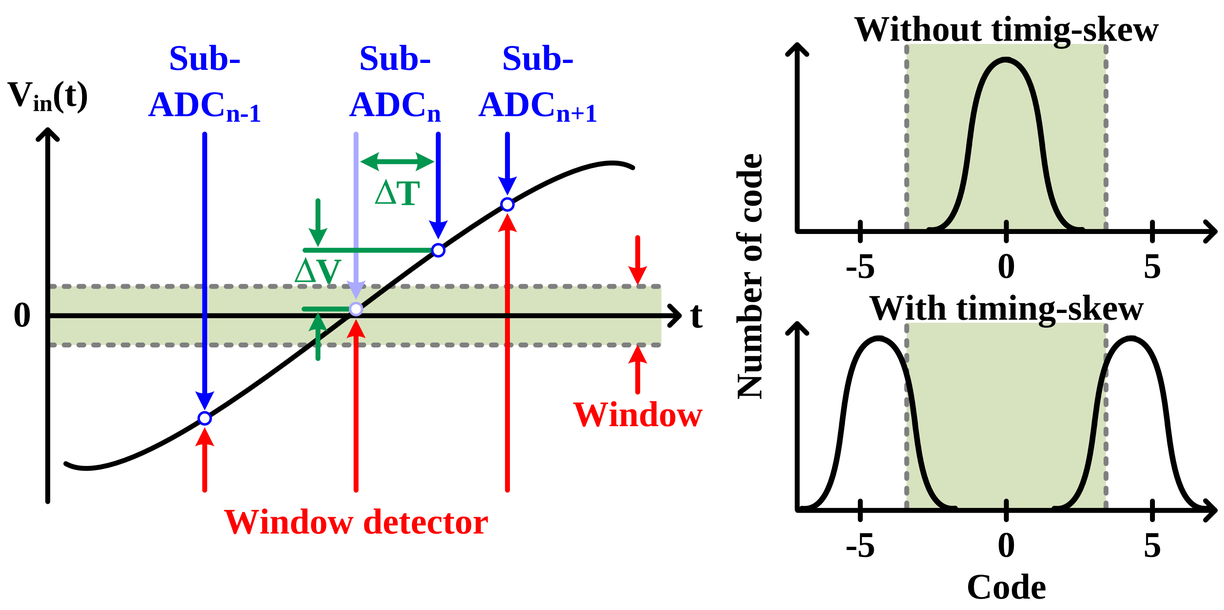

Fig. 2. Window detector-based timing-skew detection.

Proposed Timing-Skew Detection

Fig. 3 shows the concept of the proposed window detector. Fig. 3a and 3b show the input cross-coupled comparators without and with an offset (OS_{WD}), respectively. As seen in Fig. 3c and 3d, if there is no offset, the outputs of the comparators must be always opposite one another, regardless of whether the input is in the window or not. However, if there is the offset, the comparator outputs must be the same when the input falls into the window region as shown in Fig. 3c. Otherwise, if the input is out of window, the comparator outputs must be opposite to each other as described in Fig 3d. Therefore, the comparators with offset can be used as window detector and the window width is set by the offset.

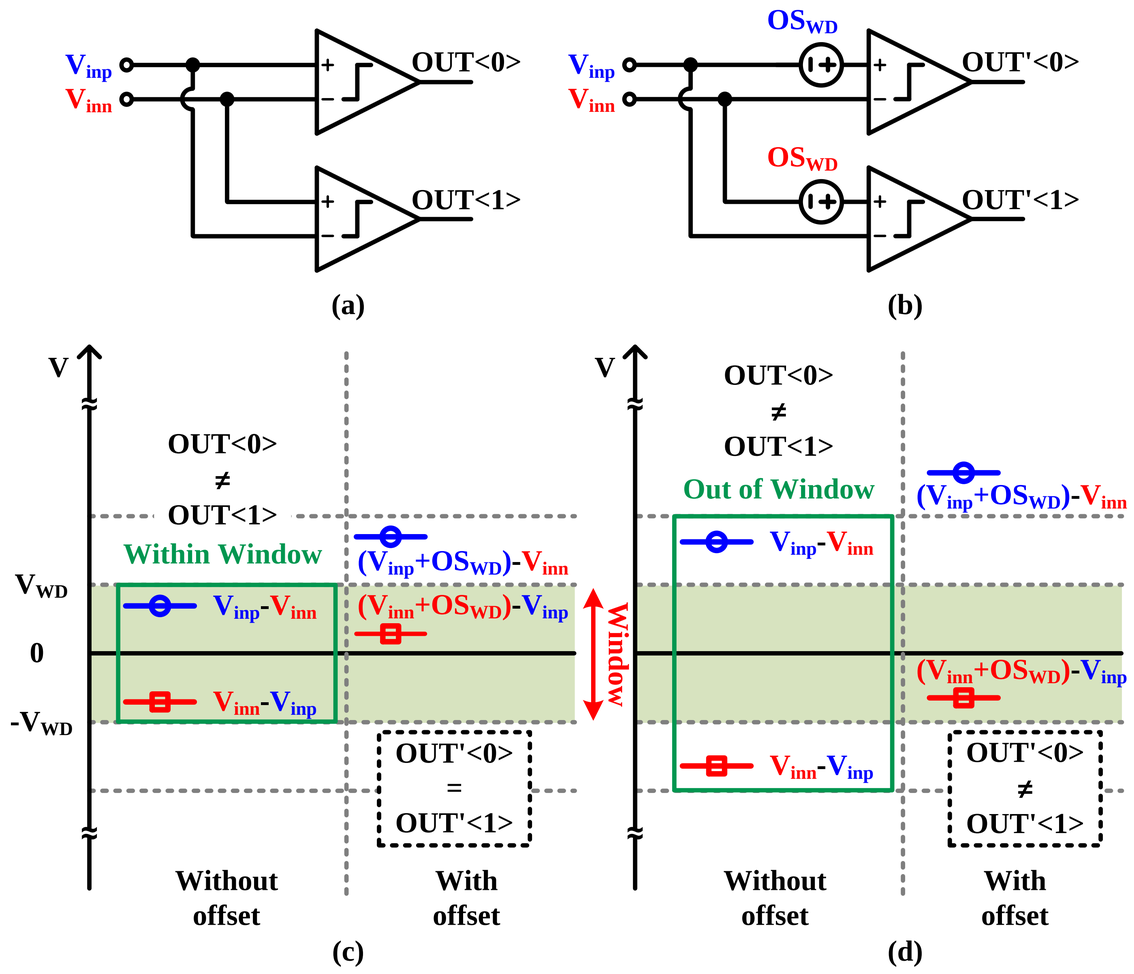

Fig. 3. Proposed timing-skew detection.

Results and Conclusion

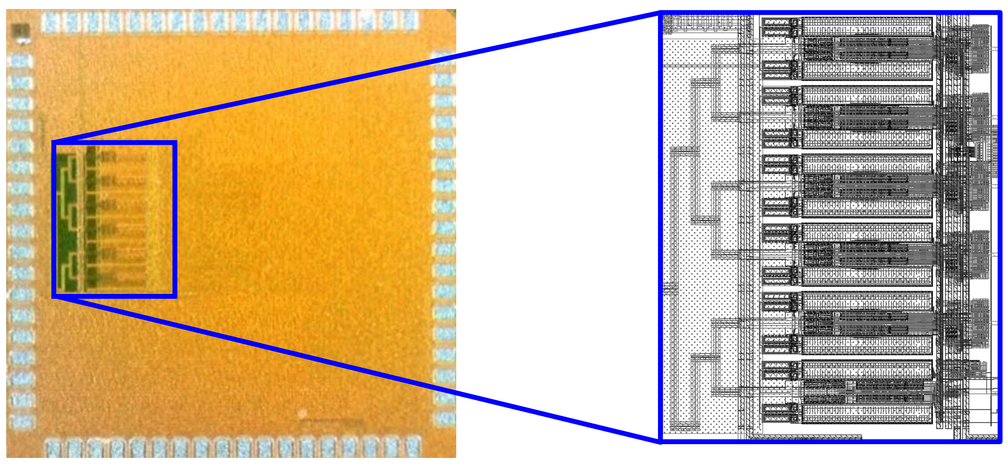

Fig. 4. Chip die photo and layout

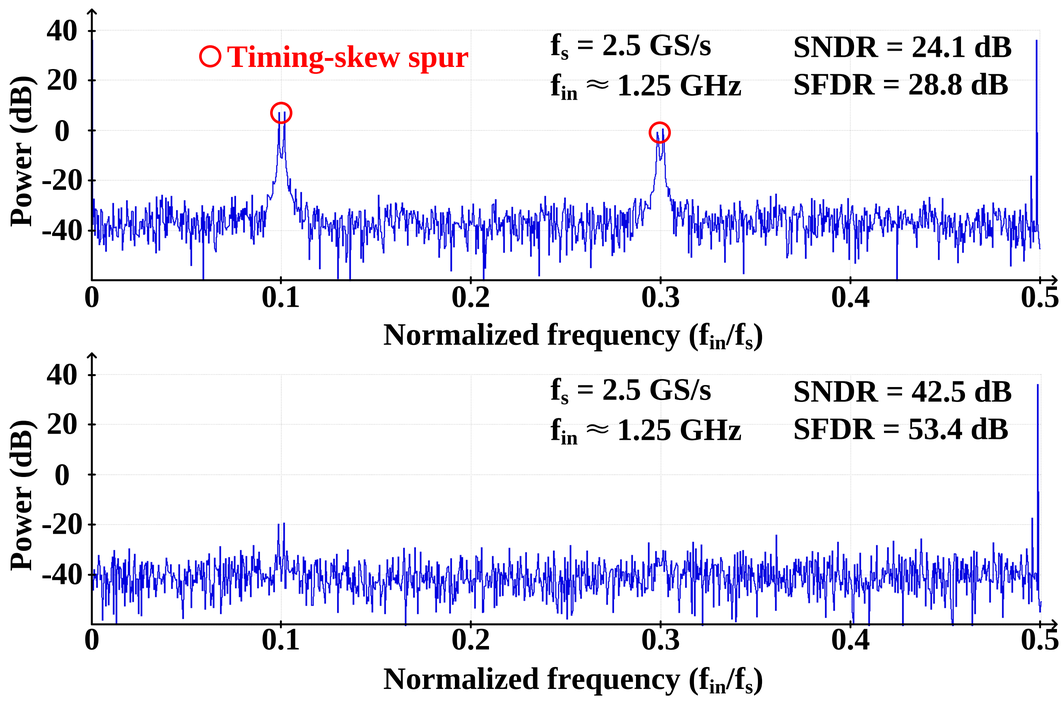

Fig. 5. Fast Fourier transform (FFT) results.

To verify the timing-skew calibration using proposed window detector, the 5-way 2.5 GS/s TI SAR ADC is fabricated in 65nm CMOS process. The proposed timing-skew calibration suppresses the timing-skew spur as shown in Fig. 5.

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